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I. SUMMARY

During the second quarter additional design calculations were made to compute the voltage capability and the current gain of the transistor. The epitaxial technique and the diffusion process were perfected. Most of the work on the encapsulation was completed.

Three designs are under consideration. The details of these designs are given in the next section. Three groups of transistors were fabricated according to Design 1 and two groups of transistors were fabricated according to Designs 2 and 3. These transistors were encapsulated. The electrical characteristics are included in Sections II and III.

author

II. PROGRESS DURING SECOND QUARTER

A. Material Preparation

The epitaxial surface requirements for the 100-amp transistors are stringent; no defects are tolerable over the entire large area active region. Small area devices can tolerate several defects since these units can be discarded. However, the presence of one defect in the 100-amp configuration would nullify the unit because of the resultant low voltage or short characteristics. It has been determined that all epitaxial defects originate at the substrate epitaxial layer interface and are dependent on surface cleanliness, substrate perfection and system purity.

1. Substrates:

The substrates used for the 100-amp devices are degenerate in that they are heavily doped with impurities. The doping level of the substrate was selected to obtain the designed saturation voltage characteristics. Heavily doped substrates inherently contain sufficient impurities to distort the crystal lattice. Distortions caused by precipitates or inclusions will not permit a sufficiently good lattice match for defect-free epitaxial growth. These distortions can be eliminated by careful selection of the parent crystal growth conditions and the type of dopant. Evaluation of the substrate material is accomplished by examination of the chemically polished surface prior to epitaxial growth. A chemically polished surface is employed for this device to insure a damage-free surface and to permit microscopic examination of the surface before growth is initiated.

2. Substrate Preparation:

Preparation of the substrate material before epitaxial growth is a deciding factor in producing defect-free epitaxial layers. Heavy metal impurities, such as aluminum or iron, are retained by the substrate after the slicing and doping operations. These can give rise to foreign

nucleation sites during the growth process. Wetting agents or solvents do not effectively remove these heavy metals. However, chemical techniques, such as reactive chloride acids, convert most heavy metals to water soluble metal chlorides and are easily removed by subsequent rinsing in deionized water.

3. Epitaxial System Purity:

Epitaxial growth perfection is also dependent on system purity, that is, the environment in which the chemical reduction of the halide takes place.

a. Gas System -- The gases used in the epitaxial process must be of good quality. The hydrogen used for the reduction is passed through a Deoro unit to remove traces of oxygen and then through a dryer to remove submicron filters to remove foreign particles before they enter the reaction chamber.

The control of the gases, the valving and piping required to mix and dilute, switching and metering are all done in a system that is leak proof. The materials of construction are of teflon, quartz, and stainless steel to maintain gas purity prior to the reaction chamber.

b. Reactor -- A horizontal RF heated epitaxial system was used for all the 100-amp device substrates (Figure 1). The susceptor is a pure grade of graphite coated with silicon carbide. The silicon carbide is deposited on the graphite under the same conditions required for epitaxial growth.

The reaction tube is of quartz and the susceptor is supported in a quartz sled. Reactor tube and susceptor loading is accomplished in a positive pressure hood to minimize dust or environmental particles from contaminating the surfaces of the slices.

c. Epitaxial Procedure -- The epitaxial procedure for the 100-amp device consists of heating the substrates to 1200°C in a filtered dry hydrogen atmosphere. Pure gaseous HCl is introduced to etch the substrates prior to growth. The reaction of HCl and silicon is the reverse of the deposition reaction and permits the removal of the last traces of work damage caused by chemical polishing.

$$4\ HCl + Si \text{ ---- } SCl_4 + 2\ H_2$$

Sufficient silicon is removed to insure a lattice match for the growth operation.

The HCl procedure is followed with a pure hydrogen treatment at 1200°C to clean out the reaction area of any chlorides which could act as nucleation sites. The collector area deposition follows for the designed thickness and the resistivity is controlled to 8-12 ohm-cm N-type. After the collector has been deposited, the system is purged with pure hydrogen at 1200°C to remove the residual traces of the gases from the collector deposition. The P^+ base layer deposition then follows to give a layer of 4-5μ of P, 0.1 ohm-cm. Gaseous dopants such as phosphine and diborane are used to control the resistivity in the epitaxial layers. After the growth of the base layer, the system is cooled for removal of the substrates.

d. Evaluation --

(1) Resistivity: The resistivity of the grown layers are determined using a three-point and a four-point probe. The collector resistivity is determined by three-point readings on a single N^+N^- deposition.

(2) Layer Thickness: The thickness of the deposited layers is determined by angle lapping and staining techniques. Interference measurements with sodium light are used to determine actual layer thicknesses.

(3) Surface Quality: Visual examination, microscopic techniques and chemical etching of the surface are used for surface evaluation. If under visual examination any defect is found in the active area of the deposited substrate, that slice is rejected, since units fabricated from slices containing poly inclusions on tetrahedrals always gave low voltages (V_{CB} of 5 - 10 volts).

The surfaces are also etched in a chromic, hydrofluoric acid, water mixture to determine the number of stacking faults present. Counts of 8-20 per cm^2 are typical.

Microscopic examination is used to determine the presence of defects not seen by the visual technique. However, yields of 90% good electrical units were achieved on those slices that passed the visual examination.

Table I compares the electrical characteristics of mesa diodes on one slice with an epitaxial collector and base with mesa diodes etched on a slice with an epitaxial collector and diffused base. Uniformity of deposition is illustrated here as well as the low leakage capabilities of the epitaxial process.

B. Emitter Design

Initially a novel design approach was considered which would take into consideration any defects formed in the crystal structure during fabrication, such as pipes and spikes, which would limit the performance of the device. The approach under investigation called for a series of individual emitters formed by oxide masking and diffusion on a single crystal. Only those emitters found to be in specification would be connected externally in order to meet the current gain and voltage requirements. Use of individual emitters on the silicon would allow considerably greater effective emitter edge length to be obtained in a given area than in the conventional interdigitated comb structure where area must be used for emitter interconnections. The individual emitters were to be stripes

formed by diffusion into silicon, each stripe being 10 mils in width separated by a base strip of 5 mils width. The total emitter edge length, when strips of this size are employed, would be 42 inches.

Unfortunately problems of encapsulation made it necessary to abandon this initial approach. Tolerances involved in using a ceramic disc to make contact to the emitter and base area of the silicon device were too fine, and the orientation of the ceramic disc within the case was nearly impossible. These technological difficulties offset any advantages that may have occurred using this design.

Another method employing the redundancy concept was developed. In this approach a series of 10-ampere modules was fabricated on a single silicon slice incorporating the original diffusion profiles, oxide masking and photoresist techniques. The best of these modules was connected in parallel to obtain 100 amperes. Each module is a separate transistor isolated from the other transistors on the slice by mesa etching. A hexagonal shape was chosen for each module. This shape had the advantage of filling the surface of a circular slice of silicon with very little waste. In addition, the opposing apexes of the hexagon offered suitable areas for contacting the base and emitter of each module.

Nineteen modules could be placed on a slice 1 1/8 inch in diameter in the manner pictured in Figure 2 . Each module has an emitter with an edge length of approximately 2.5 inches, as required for 10-ampere operation. The total array is therefore theoretically capable of operating at 190 amps. This redundancy design offers advantages in fabrication yield, gain, and saturation characteristics for the subject transistor. Difficulties were encountered in interconnection and encapsulation of the 19 module units. Due to this problem, a single 100-amp unit was designed. This is the design employed in the final transistor and is shown in Figure 3 . The design consists of 45 emitter fingers with a total emitter edge length equal to 21 inches and a total emitter contact area equal to 0.5 $(in.)^2$.

C. Fabrication

Three groups of transistors were fabricated during the second quarter. An N^- collector region and a P^+ base region were grown epitaxially in successive steps on an N^+ substrate. After depositing a layer of oxide on the base region, the emitter mask was used to expose the area for the emitter diffusion. The emitter layer was then diffused. The unit was then hard soldered to a moly disc. The emitter-base contact mask was used to expose the area for metalization. The contact area was evaporated with aluminum, and the slices were alloyed. The photographs of the various masks used for the fabrication are shown in Figures 4, 5, 6 and 7. The parameters of these transistors were:

surface concentration for the emitter diffusion = 1.5×10^{21} atoms/cm^3
concentration of the base region = 1×10^{18} atoms/cm^3
concentration of the collector region = 4×10^{14} atoms/cm^3
emitter diffusion depth = 3.3 microns
base width = 2.5 microns
intrinsic collector width = 15 microns.

The electrical characteristics of these transistors are shown in Table II.

D. Encapsulation

The contacting elements were designed so that no changes in external outline would be required.

1. Emitter:

The emitter contact consists of a Teflon washer with a thin layer of silver foil formed around it to conform with the emitter contacting surface of the basic device. The thickness of the Teflon washer was designed so that the stress-strain characteristics would allow it to flow and conform to the emitter lead and device surface, yet not so great that it would push the emitter contact area from the surface of the device. The silver foil was fashioned to allow cold flow of the Teflon.

2. Base Contact:

The base contact element consists of a nail head silver wire and Teflon locator. An important feature of the Teflon locator is the reverse chamfer at the contacting surface. This feature allows for the cold flow of the emitter contact under pressure, which in turn locks the base in place. The Teflon locator serves another important function in centering the emitter contact on the surface of the basic fusion.

In the first emitter contacts the silver was notched and formed around the Teflon cushioning pad by hand. It was very difficult to align the contacting area accurately and form the expansion arch. Tooling was designed and the remaining contacts were made by a multiple punch and die method. This method left wrinkles on the contacting surface, but it was found that these wrinkles did not adversely affect the characteristics of the device.

3. Collector:

It is very important that in designing the collector contact to keep in mind that it is through this contact that the heat generated within the basic fusion flows to be dissipated in the base and heat sink. This requires that the molybdenum mounting disc of the basic fusion and the base be in intimate contact. To enhance the intimate contact between the basic fusion and the base, a soft silver disc was placed between them. The purpose of this disc was to fill as many voids (due to lack of flatness and surface finish) as possible in both the molybdenum mounting disc and pedestal surface.

Upon examining the foil after disassembly, the imprint of the molybdenum and the base surface irregularities were clearly visible; indicating that the silver foil was performing as intended.

III. PROGRESS DURING PRESENT PERIOD

In addition to the design mentioned in the last section (Design 1) two other designs were carried out. Design 2 is identical with Design 1 except for the fact that the collector thickness is reduced to 6-8 microns. Two groups of transistors were fabricated and encapsulated according to this design and the electrical test results are shown in Table III. In Design 3 a P^- base region was grown epitaxially on an N^+ substrate and the emitter region was then diffused on the top of the base region. Three groups of transistors were fabricated and encapsulated according to this design. The parameters of these transistors are as follows:

concentration of the N^+ substrate = $1x10^{19}$ atoms/cm^3
concentration of the P^- base region = $1x10^{15}$ atoms/cm^3
thickness of the base region = 6.5 microns
surface concentration of the emitter diffusion = $1x10^{21}$ atoms/cm^3
emitter diffusion depth = 4 microns

The net impurity distribution of the three designs are given in Figures 8a, 8b and 8c. The electrical test results are shown in Table IV. The voltage and the current are within the specification of the present contract.

The high value of $V_{CE(sat)}$ for Design 3 is understandable. Because of the large difference in doping between the emitter and the base region, the value of R_{bb}, is considerable and this increases the saturation voltage. At present, efforts are being made to reduce the effect of R_{bb}'.

In addition to the three epitaxial designs, the parameters for the plain simultaneously diffused version have been calculated. Material has been acquired and processing has been initiated.

The deep diffusions required for the simultaneously diffused structure are more amenable to the mesa type. Tolerances, both surface and bulk, are critical for this approach since the bulk base width must be controlled over a large area. The emitter geometry is defined by a silicon etch for this approach and as such is less controllable than the planar epitaxial version which requires only an oxide etch.

IV. PROGRAM FOR NEXT PERIOD

During the next period some changes in the fabrication procedure for Design 3 will be made to minimize R_{bb}'. This procedure will essentially consist of diffusing a thin layer P dopant on the top of the base region with concentration slightly less than that of the emitter region. The simultaneously diffused version will also be processed and evaluated during this period. The results of this modified fabrication will be reported in the next monthly report.

V. MANHOURS EXPENDED

The following is the total manhours expended to date:

Engineers	786 hours
Technicians	769 hours

I L L U S T R A T I O N S

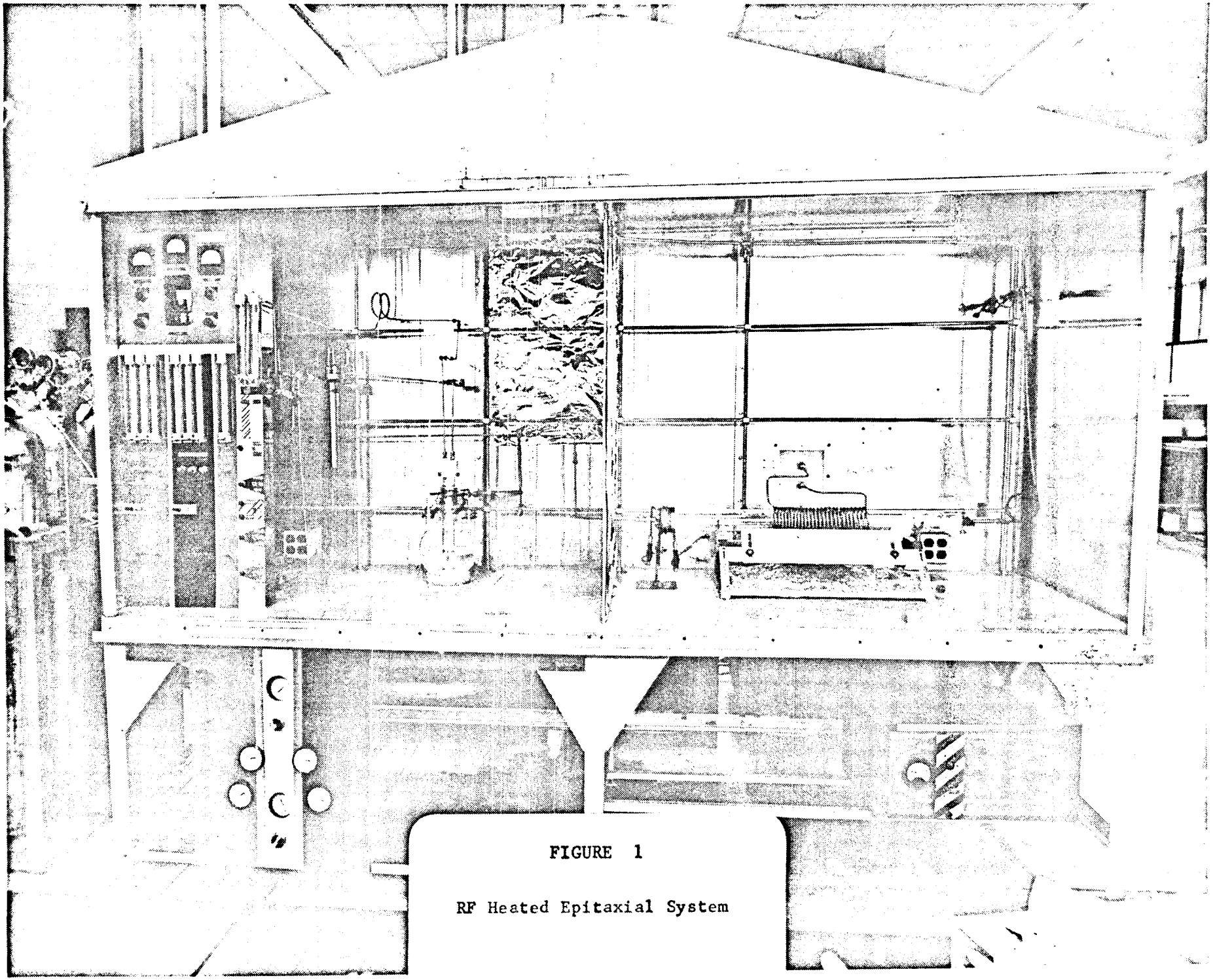

FIGURE 1

RF Heated Epitaxial System

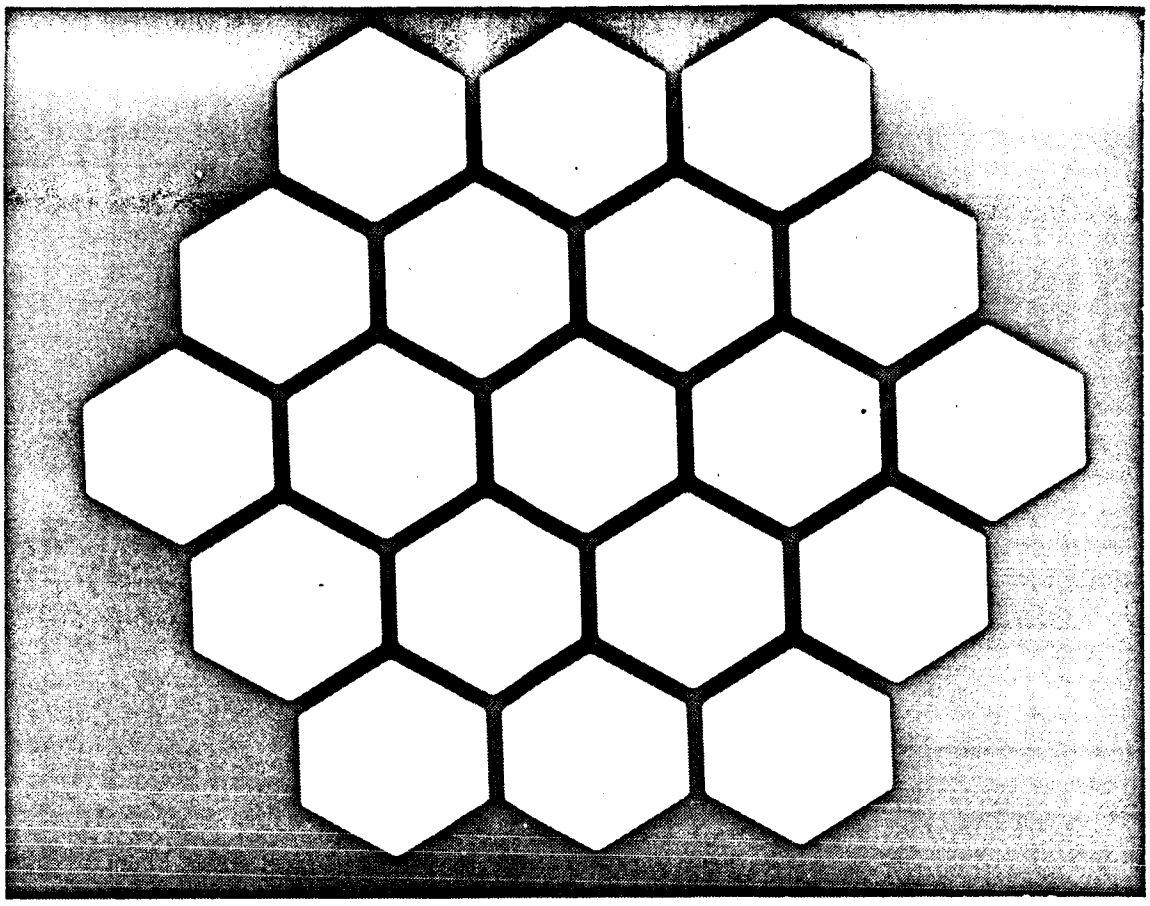

FIGURE 2

Mesa Mask

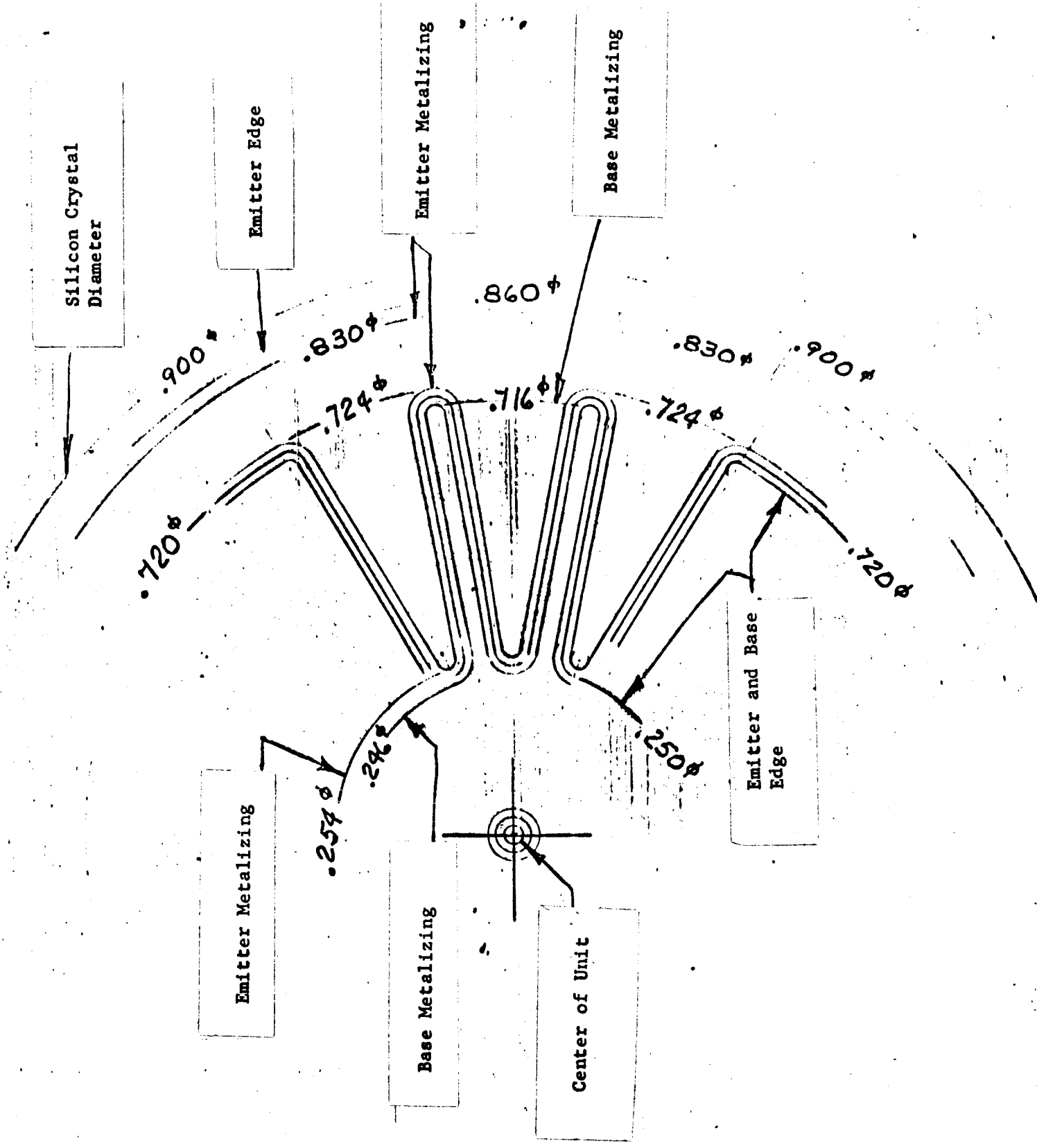

FIGURE 3

100 AMP TRANSISTOR

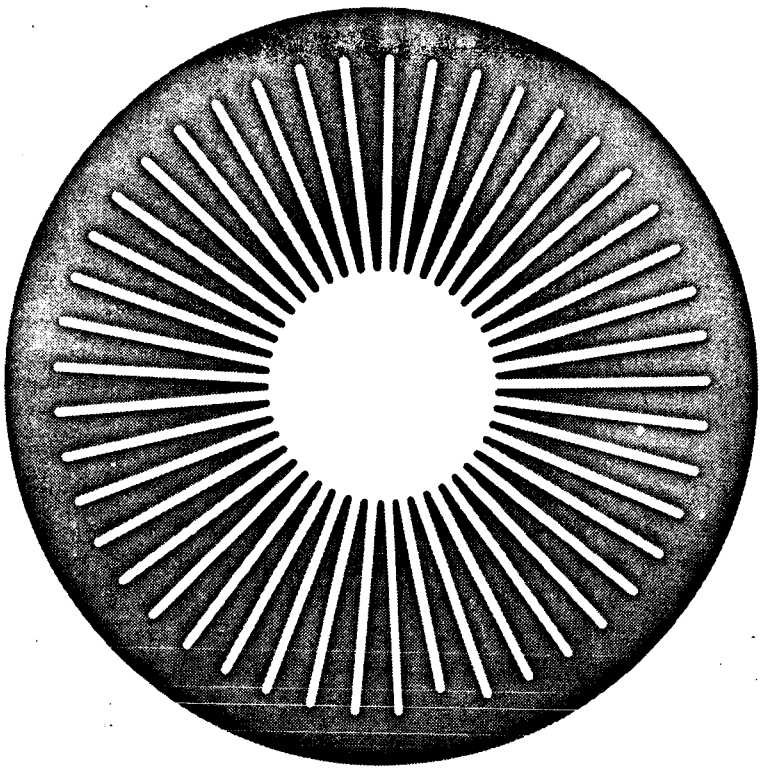

FIGURE 4

Emitter Mask

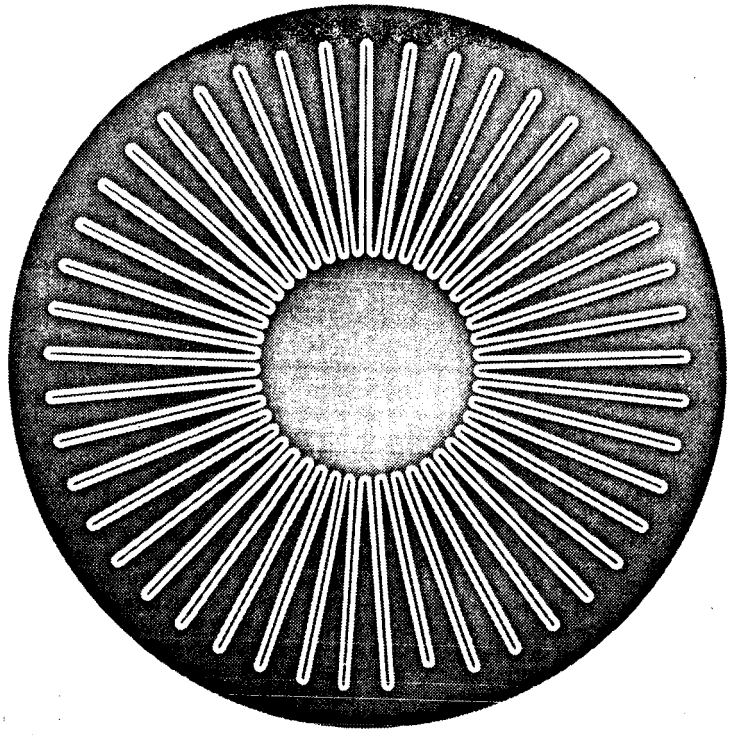

FIGURE 5

Emitter-Base Control Mask

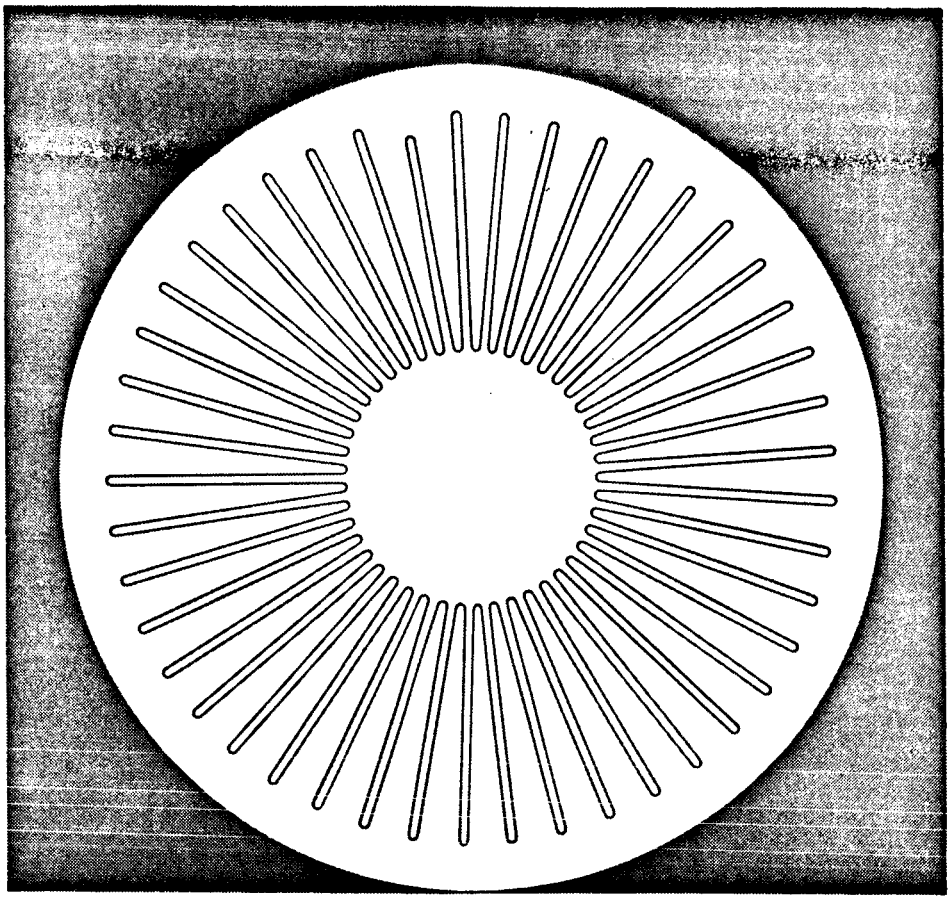

FIGURE 6

Inverse Mask

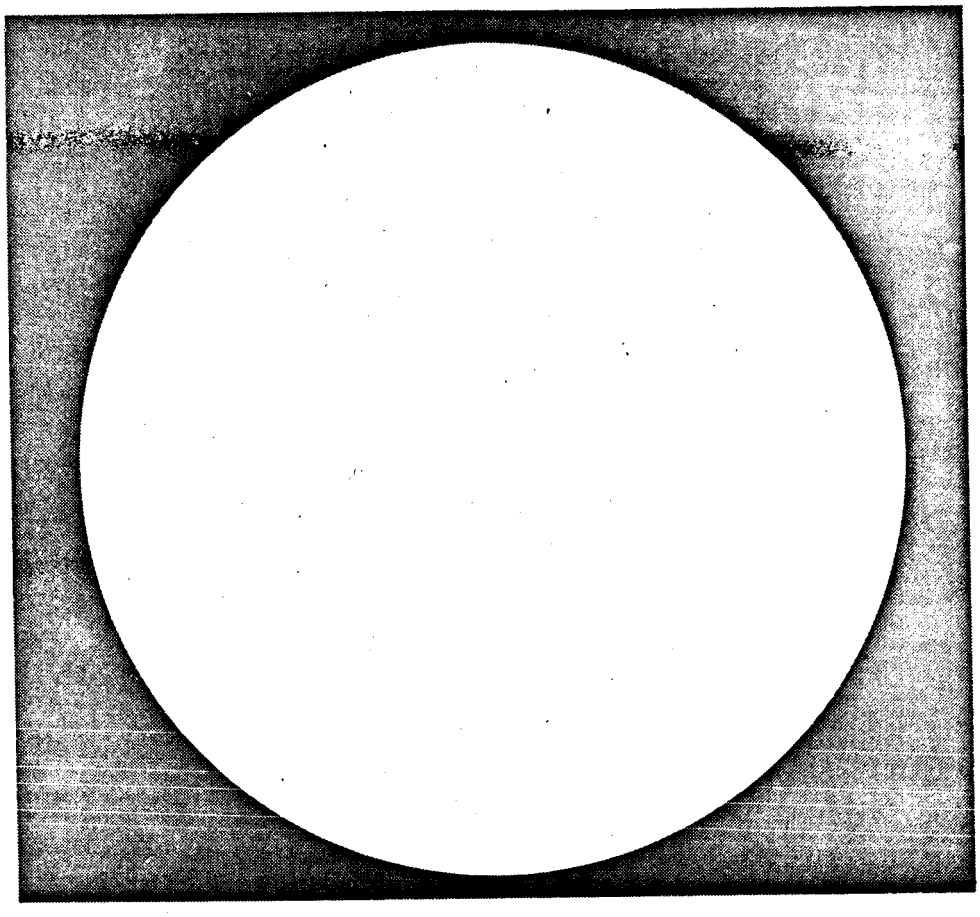

FIGURE 7

Mesa Mask

FIGURE 8a Design 1

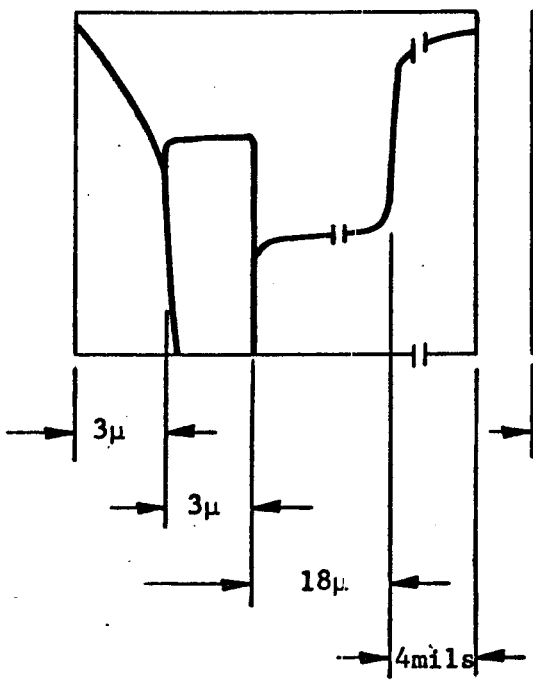

FIGURE 8b Design 2

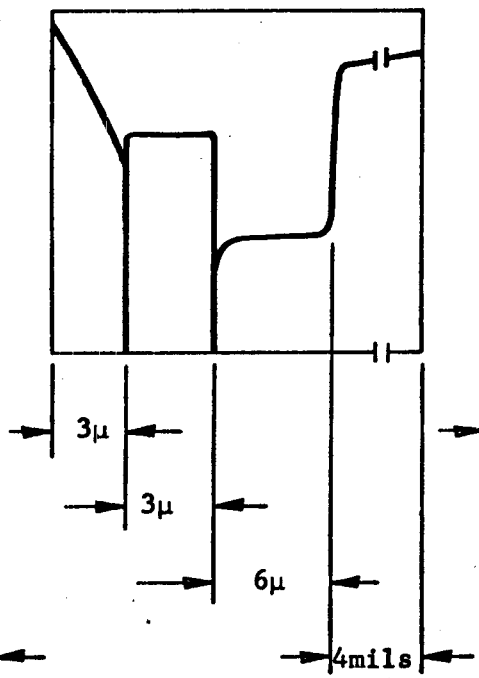

FIGURE 8c Design 3

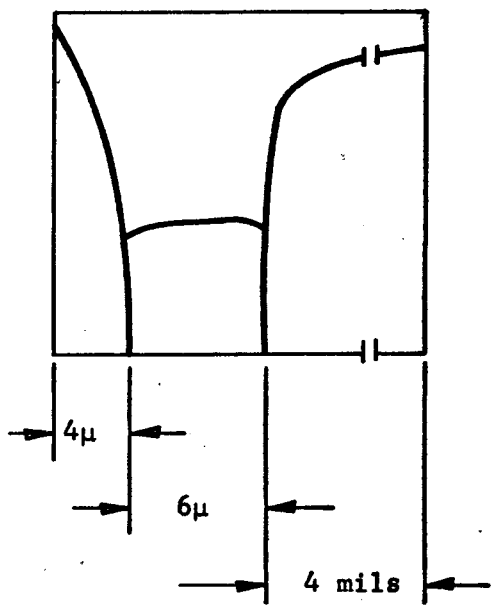

TABLE I

IV CHARACTERISTICS OF DIFFUSED AND EPITAXIAL P-N JUNCTIONS

Mesa	Epitaxial-Diffused Junction Volt/ma	Double-Epitaxial Junction Volt/ma
1	100/80	180/1
2	30/80	180/1
3	80/80	180/1
4	200/15	180/1
5	200/5	170/1
6	10/90	180/1
7	30/90	180/1
8	200/15	160/1
9	200/15	160/1
10	200/8	180/1
11	90/8	180/1
12	40/30	180/1
13	100/90	160/1
14	160/50	170/1
15	40/50	180/1
16	90/80	180/1
17	6/80	160/1
18	36/90	170/1
19	32/90	170/1

TABLE II: ELECTRICAL CHARACTERISTICS OF THE ENCAPSULATED TRANSISTORS

Unit No.	V_{EB} volt/ma	V_{CB} volt/ma	V_{CE} volt/ma	$V_{CE(sat)}$ volt at 80A	$V_{BE(sat)}$ volt at 80A	h_{FE} 20A	40A	60A	80A	100A
126-1	11/100	37/30	35/35	.34	-	13	13.3	12.5	12.3	10.6
126-2	11.5/100	46/22	40/30	.57	1.2	17.8	16.8	16	15	12.8
126-3	11/50	120/50	105/75	2.45	2.9	12	9.1	8.7	8	-
126-4	5.5/100	45/40	42/50	.67	1.1	13.5	13.5	12.5	12	10
126-5	10.5/50	140/40	120/70	2.46	2.9	11	8.5	7.6	<10	
128-1	13/50	27/100	18/500	.02	1.1	75	60	46.5	37.5	27
128-3	13.5/50	35/100	4.5/100	.42	1.1	84	70	52	42	30

TABLE III

Run No.	h_{FE} 80A	V_{CEO} V/ma	$V_{CE(sat)}$ 80A
1-1	20.5	90/100	.75V
2-1	6	50/100	> 3V
2-4	11.5	25/100	> 3V
2-5	10	50/100	> 3V
2-6	10.5	40/40	> 3V

TABLE IV

7	30	22/5	.65V
8	18.5	20/60	1.59V
9	17.5	25/10	1.2V